Planar Out-of-Phase Power Divider/Combiner for Wideband High Power Microwave Applications

Amin M. Abbosh, *Senior Member, IEEE*

***Abstract*— The design of an out-of-phase planar power divider/combiner operating over an octave frequency band is presented. The proposed device uses a modified single-section Gysel structure. The main features of the proposed device are simple and easy to package structure that does not use any slots in the ground plane, and the use of one isolation resistor that can be external to the packaging structure for efficient heat dissipation. The proposed device is suitable for high-power microwave modules and perfectly compatible with microstrip circuits. A complete design method is derived and validated. To make the device compact without jeopardizing its power capacity, a moderate meandering for the utilized transmission lines using an elliptical function is adopted. To compensate for the parasitic elements introduced in one of the signal paths due to meandering, the transmission line at the other path is elliptically tapered. The simulated and measured results of the developed device show one octave bandwidth with 180° ± 9° differential phase between the output ports and >16 dB of isolation. The final design has a compact area of <1/10 of the squared guided wavelength.**

***Index Terms*— Microstrip circuits, microwave circuits, passive circuits, power combiner, power divider.**

I. Introduction

POWER dividers/combiners are key components in many microwave circuits, such as power amplifiers, balanced mixers, modulators, and antenna array feeds to name a few [1]–[5]. As an example of the increased importance of out-of-phase power dividers, which is the topic of this paper, the recent developments in the design of microwave transceivers show that current-bleeding mixers are vital for low-noise performance [6]. Such types of mixers cannot operate without an out-of-phase power divider.

Since the most used power dividers (Wilkinson power divider/combiner [1], [7], [8]) are inherently in-phase devices, several methods were proposed to make it an out-of-phase divider/combiner. Some of those methods include using 180° phase shifters [9] or microstrip to slotline transitions [10].

The power handling capability of the devices based on the Wilkinson design is basically determined by its utilized isolation resistor. That resistor should be able to dissipate at least half the power applied to each port in case of a failure at any port. The isolation resistor of the Wilkinson device is connected internally as part of the circuit and is isolated from the ground. Thus, there is no effective way to dissipate the heat generated by that resistor especially if the device is used as part of a high-density packaged circuit. Hence, the Wilkinson design is only suitable for low-power applications.

The other design that can be used as an out-of-phase power divider/combiner is the rat-race coupler, which has a narrow-band performance. To increase its operational band, different methods are employed, such as broadside-coupled lines [11], nonplanar coupled structure [12], metamaterials [13], and cascaded structures [14]. Those methods are able to increase the bandwidth significantly. The unfortunate consequences of some of those adopted methods are, however, the reduction in the power capacity considerably because of the use of air bridges, narrows slots in the ground, narrow transmission lines, or internal lumped elements. Some of the methods also make the structure complex, costly to manufacture, and incompatible with microstrip circuits.

A notable example of rat-race couplers that are capable to handle high power is the one presented in [15]. It uses wide transmission lines of a single-section rat-rate coupler. It achieves 35% fractional bandwidth with 15 dB of isolation.

In another approach to design out-of-phase power dividers/combiners, multilayer coupled structures [16] are used [17]–[19]. In a different technique, nonplanar waveguide-based structures are used [20]. The structure proposed in [17] uses narrow slotlines, and is thus only suitable for low-power applications. The device proposed recently in [18] is designed for high-power applications that operate at two narrow bands. Although its two isolation resistors are connected to the ground, they cannot be external to the structure due to the needed stubs after the resistors. The multilayer design presented in [19] is suitable for high-power applications. It, however, has a low isolation and return loss of ∼8 dB. The nonplanar structure presented in [20] achieves one octave band, but with poor isolation, which is the norm in waveguide-based power dividers.

The other widely used power dividers/combiner is the Gysel design [21]–[23], which is inherently an in-phase device. It has the main advantage of heat-sinking capacity due to the connection of the two utilized isolation resistors to the ground plane and the possibility of making them external to the packaging structure. Thus, it is widely used in high-power microwave circuits. An extensive search in the literature shows that there are no trials to modify the Gysel's configuration to make it an out-of-phase device. If such a device can be realized, it would be an important step toward providing a

Manuscript received November 10, 2012; revised June 18, 2013; accepted August 3, 2013. Date of publication August 22, 2013; date of current version February 28, 2014. This work was supported by the Australian Research Council via the Future Fellowship under Grant FT0991479. Recommended for publication by Associate Editor M. S. Tong upon evaluation of reviewers' comments.

The author is with the School of ITEE, The University of Queensland, St Lucia 4072, Australia (e-mail: a.abbosh@uq.edu.au).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TCPMT.2013.2277587

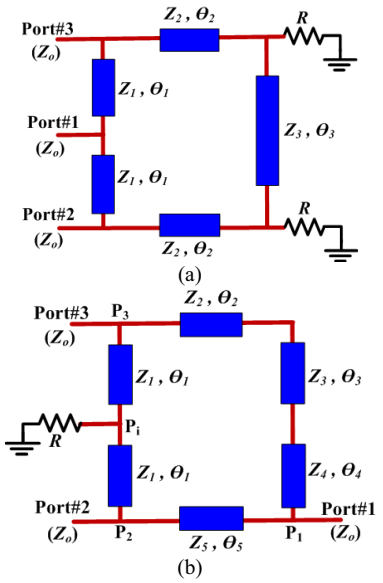


Fig. 1. Configuration of (a) Gysel divider/combiner and (b) proposed device.

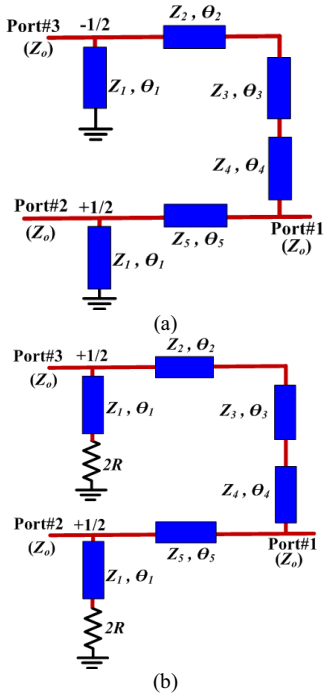


Fig. 2. Equivalent circuits of the out-of-phase power divider. (a) Odd mode. (b) Even mode.

planar out-of-phase power divider/combiner that is suitable for high-power applications and perfectly compatible with microstrip circuits.

In this paper, the Gysel structure is modified to make it an out-of-phase device. The modification also enables extending the band from 20% in the original design to 66%. One isolation resistor is needed in the modified structure. That resistor can be connected either external to the packaging structure for high-power applications or internally for low-power applications. The proposed method is validated via theory, simulations, and measurements.

II. Theory

The traditional Gysel power divide/combiner is shown in Fig. 1(a). The device has the following values for its design parameters: $Z_1 = \sqrt{2}Z_o$, $Z_2 = R = Z_o$, $Z_3 = Z_o/\sqrt{2}$, $\theta_1 = \theta_2 = 90°$, and $\theta_3 = 180°$, where $Z_o = 50\ \Omega$ is the impedance of the input and output ports.

The proposed device in this paper is derived from the Gysel structure by applying the following four modifications: 1) using only one isolation resistor that is connected at the position of Port #1; 2) moving Port #1 to the position of the lower isolation resistor; 3) replacing the half-wavelength transmission line connecting the two isolation resistors with two quarter-wavelength lines that have different impedances (Z_3, Z_4); and 4) allowing the lower arm to have a different impedance (Z_5) from the other lines. The final proposed configuration is shown in Fig. 1(b). To enable an out-of-phase power divider with proper isolation, the aforementioned modifications are designed such that: 1) the same length for the electrical path is achieved between the isolation resistor and any of the ports #2 and #3 and 2) a 180° difference in the electrical path length is realized between port #1 and the ports #2 and #3. It can be built using any type of transmission lines. In this paper, the structure is realized using microstrip lines. The structure and the three feeding ports are placed at the top layer of a printed circuit board, whereas the ground plane is located at the bottom layer. The structure does not need the use of slotted ground. Thus, it is perfectly compatible with microstrip circuits. In addition, it does not need any narrow lines or lumped elements. Knowing that its isolation resistor is connected to the ground and can be external to the structure, the proposed device is thus suitable for high-power applications. The only limit on its power capacity is the normal limitation of the utilized technology in its implementations. For example, if the printed circuit technology is used, the power handling capability will be defined by the type and dimensions of the dielectric substrate, and type and thickness of the conductive material.

The proposed structures in Fig. 1(b) can be analyzed using the even-odd mode approach. In the odd mode, the voltages at the points P_2 and P_3 of the structure shown in Fig. 1(b) should be of equal magnitude and out-of-phase. In this case, the point P_i at the connection of the isolation resistor is at virtual zero potential. Thus, the equivalent circuit for the odd-mode excitation is shown in Fig. 2(a). In the even mode, the voltages at the points P_2 and P_3 should be of equal magnitude and phase. In this case, the point P_i is virtually open circuit. Thus, the equivalent circuit for the even-mode excitation is shown in Fig. 2(b). The odd-even mode circuits can be analyzed using the ABCD matrix. In the following analysis, it is assumed that the isolation resistor $R = 50\ \Omega$, which is the available standard for high power terminations. It is also assumed that the length of each of the utilized transmission lines is quarter wavelength, i.e., $\theta_1 = \theta_2 = \theta_3 = \theta_4 = \theta_4 = 90°$.

Because of the asymmetry of the circuits in Fig. 2, they cannot be analyzed directly using the conventional approach that isolates the circuit connecting Port #2 to Port #1 from the

circuit connecting Port #3 to Port #1. Instead, the following method, which is based on applying the superposition theory and the conservation of energy principle on the circuits of Fig. 2, is used. The S-parameters of the device can be calculated from the odd- and even-mode reflection and transmission coefficients of the two ports (Port #2 and #3) that are excited by the odd- and even-mode excitations shown in Fig. 2 according to the following equations:

$$S_{12} = S_{21} = 0.5(\mathrm{T}_{21o} + \mathrm{T}_{21e} - \mathrm{T}_{31o} + \mathrm{T}_{31e}) \quad (1)$$

$$S_{13} = S_{31} = 0.5(\mathrm{T}_{31o} + \mathrm{T}_{31e} - \mathrm{T}_{21o} + \mathrm{T}_{21e}) \quad (2)$$

$$S_{22} = 0.5(\Gamma_{22o} + \Gamma_{22e} - \mathrm{T}_{32o} + \mathrm{T}_{32e}) \quad (3)$$

$$S_{33} = 0.5(\Gamma_{33o} + \Gamma_{33e} - \mathrm{T}_{23o} + \mathrm{T}_{23e}) \quad (4)$$

$$S_{32} = S_{23} = 0.5(\mathrm{T}_{32o} + \mathrm{T}_{32e} - \Gamma_{22o} + \Gamma_{22e}) \quad (5)$$

$$|S_{11}| = \sqrt{1 - \left(|S_{12}|^2 + |S_{13}|^2\right)}. \quad (6)$$

Γ_{22o}, Γ_{22e}: reflection coefficients at Port #2 for the odd and even modes, Γ_{33o}, Γ_{33e}: reflection coefficients at Port #3 for the odd and even modes, T_{21o},T_{21e}: transmission coefficients from Port #2 to Port #1 for the odd and even modes, T_{31o}, T_{31e}: transmission coefficients from Port #3 to Port #1 for the odd and even modes, and $\mathrm{T}_{23o}(= \mathrm{T}_{32o})$, $\mathrm{T}_{23e}(\mathrm{T}_{32e})$: transmission coefficients from Port #2 to Port #3, and vice versa, for the odd and even modes. Those coefficients are calculated using the equations (A1–A16) that are based on the ABCD matrices as explained in the Appendix.

The aforementioned equations can be solved using an iterative code in MATLAB depending on the design requirements. To achieve an ideal performance at a certain frequency, the characteristic impedances of the utilized quarter-wavelength transmission lines can be found from (1)–(5) as

$$Z_5 = \sqrt{2}Z_o; \quad \frac{Z_2 Z_4}{Z_3} = \sqrt{2}Z_o; \quad Z_1 = \sqrt{2}Z_o. \quad (7)$$

Assuming that $Z_2 = Z_4$ and $Z_o = 50\ \Omega$, the calculated performance of the out-of-phase power divider using (7) in (1)–(5) at the frequency band from, e.g., 4 to 8 GHz is shown in Fig. 3(a). It is obvious that the four parameters (S_{11}, S_{22}, S_{33}, and S_{23}) have zeros at the design frequency which is the center frequency (6 GHz). This result is a clear indication that the three ports of the power divider are perfectly matched and the two output ports are perfectly isolated at the design frequency. The power is equally divided between the two output ports ($S_{21} = S_{31} = -3$ dB at 6 GHz) that are out-of-phase with each other. The calculated performance using the derived model is also verified using the software Agilent ADS and it gives exactly the same performance shown in Fig. 3(a).

If the performance is inspected across the whole one octave band, it is clear from Fig. 3(a) that the return loss at the three ports of the device is ~8 dB especially at the lower and upper edges of the band. The isolation between the two output ports is >13 dB, and the differential phase between the signals at the two output ports is 180° ± 18°. The overall performance thus needs to be improved.

To get the values of the design parameters for a wideband performance, there is a need to set a certain design criteria and then to find the design parameters using the derived model

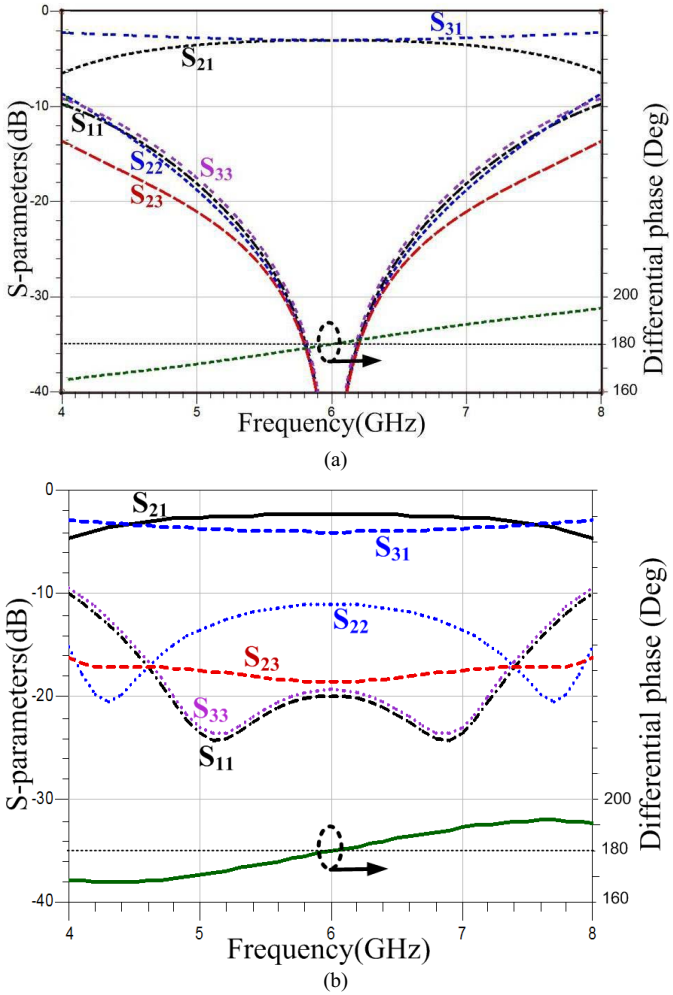
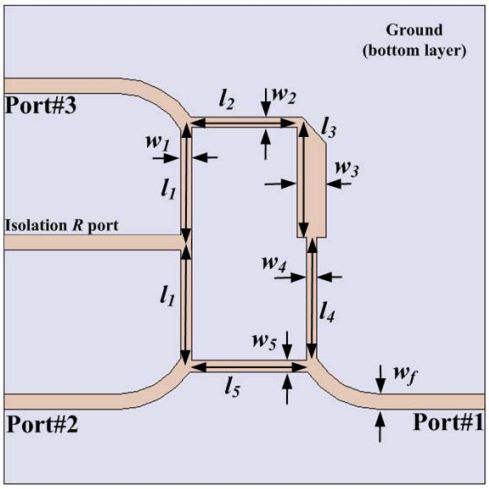


Fig. 3. Performance of the out-of-phase power divider with design parameters calculated for (a) ideal performance at the center frequency and (b) acceptable performance across one octave band.

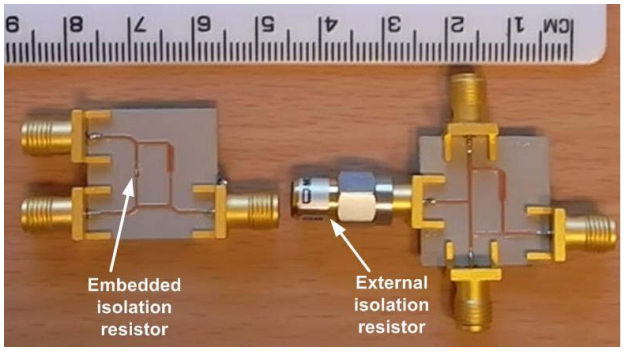
(1)–(5). As an example that meets the industrial requirements, it is assumed that the device should have >15 dB of isolation between its output ports and >10 dB of return loss at the three ports across an octave bandwidth. Since the design equations (1)–(5) and (A1)–(A16) that relate the design parameters with the required performance are nonlinear, the iterative approach is used to find their solution. To avoid using very high or low impedance values for the utilized transmission lines, the iterative solution is restricted to meet the condition $0.5Z_o \le Z_i \le 2Z_o$, where i refers to the impedance number. The other conditions on the solution are $|S_{32}|_{dB} \le -15$, $|S_{11}|_{dB} \le -10$, $|S_{22}|_{dB} \le -10$, and $|S_{33}|_{dB} \le -10$. It is possible to show that the solution that meets the above conditions is

$$Z_1 = Z_5 = 50\ \ \Omega;\ Z_2 = Z_4 = 60\Omega;\ Z_3 = 40\Omega. \quad (8)$$

It is possible also to solve (1)–(5) for other design requirements. For example, some applications may require >15 dB of both return loss and isolation. In this case, solving the aforementioned equations can be realized across >50% fractional bandwidth.



(a)



(b) (c)

Fig. 4. (a) Proposed device. (b) and (c) Two developed prototypes.

TABLE I
CALCULATED AND OPTIMIZED DIMENSIONS (mm) OF FINAL DESIGN

Para.	Cal.	Opt.	Para.	Cal.	Opt.
w_1	0.6	0.55	l_1	4.8	5.1
w_2	0.4	0.44	l_2	4.8	5
w_3	1	1	l_3	4.7	5
w_4	0.4	0.38	l_4	4.8	5
w_5	0.6	0.65	l_5	4.8	5

The calculated performance using (8) in the model (1)–(5) is shown in Fig. 3(b). The results show that the isolation is better than 15 dB and the differential phase is 180° ± 10° across an octave bandwidth. If this result is compared with that obtained when the set of parameters are calculated for an optimum performance at the center frequency [Fig. 3(a)], it becomes clear that the improvement in the performance is significant at the cost of sacrificing the excellent performance at the center of the band.

III. RESULTS AND DISCUSSION

Starting from the calculated design parameters of the proposed device for a wideband performance, the structure is optimized using the full-wave electromagnetic simulator

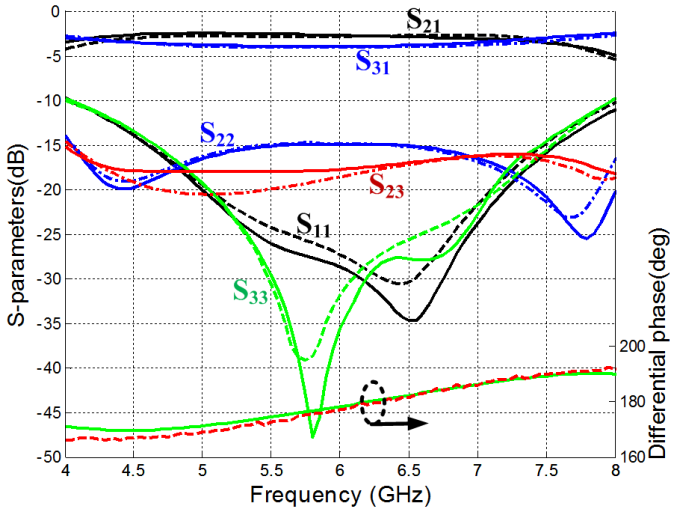


Fig. 5. Measured and simulated performance of the out-of-phase power divider. Solid lines: simulations.

HFSS. The structure used in the simulations is shown in Fig. 4(a). The target in the optimization is to achieve better than 15 dB of isolation between the two output ports, and a maximum deviation in the phase of ± 10° across one octave bandwidth (4–8 GHz). The dimensions in (mm) for the calculated impedances after using the microstrip design equations are listed in Table I together with the final optimized parameters. The optimized width of the feeding ports (w_f) is 0.65 mm. A good agreement between the calculated and optimized dimensions is clear from these values. The substrate Rogers RT6010 (thickness = 0.635 mm and dielectric constant = 10.2) is assumed. To reduce the undesired effects of the bend at the end of the wide transmission line representing Z_3, the junction between the lines representing Z_3 and Z_2 is mitered properly, as shown in Fig. 4(a).

Two prototypes of the proposed device are developed [Fig. 4(b) and (c)] and tested. The two possible ways to connect the isolation resistor are used. In the first approach that can be used for low-power applications, a chip resistor is inserted between the top layer and the group plane at the bottom layer as shown in Fig. 4(b). In the second approach, the isolation resistor is connected outside the divider's structure using a 50-Ω transmission line as shown in Fig. 4(c). This method is suitable for high-power applications as the isolation resistor can be attached to a suitable heat sink outside the structure. It is noted that the performance of the two devices is almost the same. Thus, the performance of only one of them (with an external isolation resistor) is included in this paper.

The simulated and measured performances of the designed device are shown in Fig. 5. The simulated differential phase between the two output ports is 180° ± 9°, whereas the measured differential phase shift is 180° ± 11° across the band from 4 to 8 GHz. The power is equally divided between the two output ports with a maximum amplitude imbalance of 1 dB across the band from 4 to 7.8 GHz. The measured and simulated isolation between the two output ports is > 15 dB across the whole investigated band from 4 to 8 GHz. The return losses for the three ports of the device are > 10 dB

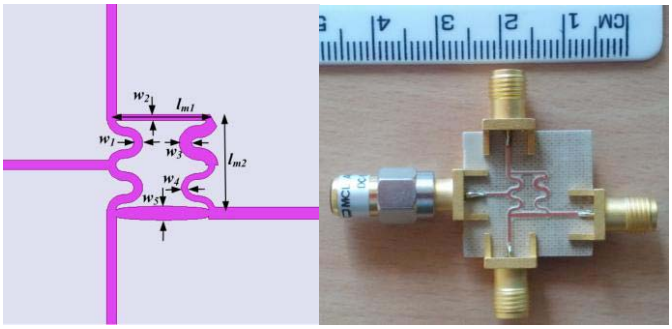


Fig. 6. Diagram and photo of the meandered/tapered structure.

for the one octave band. There is generally a good agreement between the simulated and measured results.

It is also interesting to compare the final optimized performance (Fig. 5) with the performance calculated using the derived model for the initially calculated design parameters [Fig. 3(b)]. Since the optimized values of the design parameters are not far from the initial values, the general behavior of all the S-parameters agree reasonably well with initial predictions.

Since the interior space of the device is blank and not used, the structure can be moderately meandered to reduce its size without sacrificing its power capacity. The target in the meandering is to make the side length of the structure around a quarter wavelength. Thus, only the transmission lines of lengths (l_1, l_3, and l_5) in Fig. 4(a) are meandered using elliptical shaped lines. The meandering in the lines of length l_1 has the same effect on the two signal paths (from Port #1 to Ports #2 and #3). However, the meandering process on l_3 and l_5 introduces parasitic elements on the link from Port #1 to Port #3. Those elements cause deterioration in the differential phase performance. To compensate for that effect, the transmission line connecting Port #1 to Port #2 is tapered slightly using an elliptical function. The final structure is shown in Fig. 6. Because of the meandering process, the structure needs an additional optimization starting from the initial dimensions calculated for the impedance values of $Z_1 = Z_5 = 50\ \Omega$, $Z_2 = Z_4 = 60\ \Omega$, and $Z_3 = 40\ \Omega$ that are estimated for wideband performance in the previous section. It is found that the optimized dimensions in (mm) for the meandered structure to achieve one octave band are $w_1 = 0.53$, $w_2 = 0.35$, $w_3 = 0.75$, $w_4 = 0.37$, and $w_5 = 0.4$ at the ends, and 0.9 at the center. The side lengths of the device excluding the feeding ports are $l_{m1} = 5.3$ and $l_{m2} = 5.9$. The area of the meandered device excluding the four feeders represents $\sim 60\%$ of the nonmeandered structure [Fig. 4(a)]. Although an excessive meandering can be used to achieve an area of $< 30\%$ of the nonmeandered area, it is not sought here to avoid jeopardizing the power handling capability of the device.

The miniaturized device is fabricated (Fig. 6) and tested. The simulated and measured performances are shown in Fig. 7. It is clear that despite the reduction in size, the overall performance meets the design criteria with $> 66\%$ fractional bandwidth assuming the 16-dB isolation as a reference. The

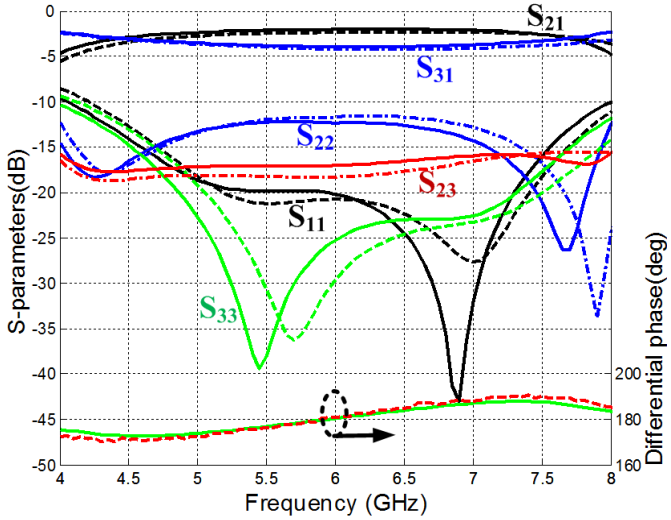


Fig. 7. Measured and simulated performance of the meandered compact out-of-phase power divider. Solid lines: simulations.

TABLE II
COMPARISON BETWEEN PERFORMANCE OF PROPOSED OUT-OF-PHASE DIVIDER/COMBINER AND PUBLISHED PLANAR HIGH POWER DESIGNS

Ref#	% BW	Isolation (dB)	Area per λ_g^2	Microstrip compatibility
[14]	50	25	0.1	Yes
[15]	35	15	0.12	Yes
[18]	Dual-band 14	15	0.45	No
[19]	110	8	0.4	No
This work	66	16	0.08	Yes

differential phase between the two output ports is $180° \pm 9°$ across the band from 4 to 8 GHz. To clarify the effect of the $\pm 9°$ phase imbalance on the overall performance, it is possible to show that it would cause <0.03 dB additional insertion loss when the device is used as a power combiner.

The performance of the proposed device is compared with other recently published planar out-of-phase designs of high power capability as shown in Table II. It is possible to claim that the proposed device has the widest fractional bandwidth assuming the 15-dB isolation as the reference. The device included in this paper has also the smallest size (with respect to the guided wavelength) and is fully compatible with microstrip circuits.

The simple structure of the proposed device, the need for only one isolation resistor that can be connected outside the packaging structure, its perfect compatibility with microstrip circuits, and the wideband performance make it good candidate for high-power microstrip circuits.

IV. CONCLUSION

A planar out-of-phase power divider/combiner of modified single-section Gysel design has been presented. Since the isolation resistor in the proposed structure can be connected externally using a suitable transmission line, the proposed device is specifically suitable for high-power microwave appli-

cations. It is also fully compatible with microstrip circuits. The presented results of the developed device show >16 dB of isolation with less than ± 9° of phase imbalance across > 66% fractional bandwidth.

APPENDIX

In the following analysis, the odd- and even-mode circuits of Fig. 2 are used. The impedances of different transmission lines and the isolation resistor are taken here as normalized values with respect to the standard port impedance (50 Ω).

A. Calculation of Γ_{22o},Γ_{22e}, T_{21o}, and T_{21e}

For this case, Port #3 is terminated in matched load. The equivalent ABCD matrix is the multiplication of the cascaded matrices representing different circuit elements connected between Port #2 and Port #1 including the effect of the terminated Port #3.

Odd mode:

$$[M_{2o}] = \begin{bmatrix} M_{2o}(1,1) & M_{2o}(1,2) \\ M_{2o}(2,1) & M_{2o}(2,2) \end{bmatrix} = [m1] * [m2] * [m3] \tag{A-1}$$

$$\Gamma_{22o} = \frac{M_{2o}(1,1) + M_{2o}(1,2) - M_{2o}(2,1) - M_{2o}(2,2)}{M_{2o}(1,1) + M_{2o}(1,2) + M_{2o}(2,1) + M_{2o}(2,2)} \tag{A-2}$$

$$T_{21o} = \frac{2}{M_{2o}(1,1) + M_{2o}(1,2) + M_{2o}(2,1) + M_{2o}(2,2)} \tag{A-3}$$

where $[m1] = \begin{bmatrix} 1 & 0 \\ 1/(jz_1\tan\theta) & 1 \end{bmatrix}$

$[m2] = \begin{bmatrix} \cos\theta & jz_5\sin\theta \\ j\sin\theta/z_5 & \cos\theta \end{bmatrix}$; $[m3] = \begin{bmatrix} 1 & 0 \\ 1/z_{io3} & 1 \end{bmatrix}$

$$z_{io3} = \frac{z_4(z_c + jz_4\tan\theta)}{z_4 + jz_c\tan\theta}; \quad z_c = \frac{z_3(z_b + jz_3\tan\theta)}{z_3 + jz_b\tan\theta};$$
$$z_b = \frac{z_2(z_a + jz_2\tan\theta)}{z_2 + jz_a\tan\theta}; \quad z_a = \frac{jz_1\tan\theta}{1 + jz_1\tan\theta}.$$

Even mode:

$$[M_{2e}] = \begin{bmatrix} M_{2e}(1,1) & M_{2e}(1,2) \\ M_{2e}(2,1) & M_{2e}(2,2) \end{bmatrix} = [m4] * [m2] * [m5] \tag{A-4}$$

$$\Gamma_{22e} = \frac{M_{2e}(1,1) + M_{2e}(1,2) - M_{2e}(2,1) - M_{2e}(2,2)}{M_{2e}(1,1) + M_{2e}(1,2) + M_{2e}(2,1) + M_{2e}(2,2)} \tag{A-5}$$

$$T_{21e} = \frac{2}{M_{2e}(1,1) + M_{2e}(1,2) + M_{2e}(2,1) + M_{2e}(2,2)} \tag{A-6}$$

where $[m4] = \begin{bmatrix} 1 & 0 \\ (z_1 + j2\tan\theta)/(z_1(2 + jz_1\tan\theta)) & 1 \end{bmatrix}$;

$[m5] = \begin{bmatrix} 1 & 0 \\ 1/z_{ie3} & 1 \end{bmatrix}$;

$$z_{ie3} = \frac{z_4(z_c + jz_4\tan\theta)}{z_4 + jz_c\tan\theta}; \; z_c = \frac{z_3(z_b + jz_3\tan\theta)}{z_3 + jz_b\tan\theta};$$
$$z_b = \frac{z_2(z_a + jz_2\tan\theta)}{z_2 + jz_a\tan\theta}; \; z_a = \frac{z_1(2 + jz_1\tan\theta)}{3z_1 + j(2 + z_1^2)\tan\theta}.$$

B. Calculations of Γ_{33o}, Γ_{33e}, T_{31o}, and T_{31e}

In this case, Port #2 is terminated in matched load. The equivalent ABCD matrix is the multiplication of the cascaded matrices representing different circuit elements connected between Port #3 and Port #1 including the effect of the terminated Port #2.

Odd mode:

$$[M_{3o}] = \begin{bmatrix} M_{3o}(1,1) & M_{3o}(1,2) \\ M_{3o}(2,1) & M_{3o}(2,2) \end{bmatrix} = [m1] * [m6] * [m7] * [m8] * [m9] \tag{A-7}$$

$$\Gamma_{33o} = \frac{M_{3o}(1,1) + M_{3o}(1,2) - M_{3o}(2,1) - M_{3o}(2,2)}{M_{3o}(1,1) + M_{3o}(1,2) + M_{3o}(2,1) + M_{3o}(2,2)} \tag{A-8}$$

$$T_{31o} = \frac{2}{M_{3o}(1,1) + M_{3o}(1,2) + M_{3o}(2,1) + M_{3o}(2,2)} \tag{A-9}$$

where

$$[m6] = \begin{bmatrix} \cos\theta & jz_2\sin\theta \\ j\sin\theta/z_2 & \cos\theta \end{bmatrix};$$
$$[m7] = \begin{bmatrix} \cos\theta & jz_3\sin\theta \\ j\sin\theta/z_3 & \cos\theta \end{bmatrix};$$

$[m8] = \begin{bmatrix} \cos\theta & jz_4\sin\theta \\ j\sin\theta/z_4 & \cos\theta \end{bmatrix}$; $[m9] = \begin{bmatrix} 1 & 0 \\ 1/z_{io2} & 1 \end{bmatrix}$

$$z_{io2} = \frac{z_5(z_b + jz_5\tan\theta)}{z_5 + jz_b\tan\theta}; \quad z_b = \frac{jz_1\tan\theta}{1 + jz_1\tan\theta}.$$

Even mode:

$$[M_{3e}] = \begin{bmatrix} M_{3e}(1,1) & M_{3e}(1,2) \\ M_{3e}(2,1) & M_{3e}(2,2) \end{bmatrix} = [m4] * [m6] * [m7] * [m8] * [m10] \tag{A-10}$$

$$\Gamma_{33e} = \frac{M_{3e}(1,1) + M_{3e}(1,2) - M_{3e}(2,1) - M_{3e}(2,2)}{M_{3e}(1,1) + M_{3e}(1,2) + M_{3e}(2,1) + M_{3e}(2,2)} \tag{A-11}$$

$$T_{31e} = \frac{2}{M_{3e}(1,1) + M_{3e}(1,2) + M_{3e}(2,1) + M_{3e}(2,2)} \tag{A-12}$$

where $[m10] = \begin{bmatrix} 1 & 0 \\ 1/z_{ie2} & 1 \end{bmatrix}$;

$$z_{ie2} = \frac{z_5(z_b + jz_5\tan\theta)}{z_5 + jz_b\tan\theta}; \quad z_b = \frac{z_1(2 + jz_1\tan\theta)}{3z_1 + j(2 + z_1^2)\tan\theta}.$$

C. Calculations of $T_{23o}(= T_{32o})$ and $T_{23e}(= T_{32e})$

In this case, Port #1 is terminated in matched load. The equivalent ABCD matrix is the multiplication of the cascaded matrices representing the circuit elements from Port#2 to Port #3.

Odd mode:

$$[M_{23o}] = \begin{bmatrix} M_{23o}(1,1) & M_{23o}(1,2) \\ M_{23o}(2,1) & M_{23o}(2,2) \end{bmatrix} = [m1] * [m2] * [m11] * [m8] * [m7] * [m6] * [m1] \tag{A-13}$$

where $[m11] = \begin{bmatrix} 1 & 0 \\ 1 & 1 \end{bmatrix}$

$$T_{32o} = T_{23o} = \frac{2}{M_{32o}(1,1) + M_{32o}(1,2) + M_{32o}(2,1) + M_{32o}(2,2)}. \tag{A-14}$$

Even mode:

$$[M_{23e}] = \begin{bmatrix} M_{23e}(1,1) & M_{23e}(1,2) \\ M_{23e}(2,1) & M_{23e}(2,2) \end{bmatrix} = [m4] * [m2] * [m11] * [m8] * [m7] * [m6] * [m4] \tag{A-15}$$

$$T_{32e} = T_{23e} = \frac{2}{M_{32e}(1,1) + M_{32e}(1,2) + M_{32e}(2,1) + M_{32e}(2,2)}. \tag{A-16}$$

REFERENCES

[1] A. Genc and R. Baktur, "Dual- and triple-band Wilkinson power dividers based on composite right- and left-handed transmission lines," *IEEE Trans. Compon. Packag. Manuf. Technol.*, vol. 1, no. 3, pp. 327–334, Mar. 2011.

[2] M. Bialkowski, A. Abbosh, and N. Seman, "Compact microwave six-port vector voltmeters for ultra-wideband applications," *IEEE Trans. Microw. Theory Tech.*, vol. 55, no. 10, pp. 2216–2223, Oct. 2007.

[3] B. Khatib, T. Djerafi, and K. Wu, "Substrate-integrated waveguide vertical interconnects for 3-D integrated circuits," *IEEE Trans. Compon. Packag. Manuf. Technol.*, vol. 2, no. 9, pp. 1526–1535, Sep. 2012.

[4] A. Abbosh, "Multilayer inphase power divider for UWB applications," *Microw. Opt. Tech. Lett.*, vol. 50, no. 5, pp. 1402–1405, 2008.

[5] G. Carchon, K. Vaesen, S. Brebels, W. De Raedt, E. Beyne, and B. Nauwelaers, "Multilayer thin-film MCM-D for the integration of high-performance RF and microwave circuits," *IEEE Trans. Compon. Packag. Manuf. Technol.*, vol. 24, no. 3, pp. 510–519, Mar. 2001.

[6] Y. Lin, J. Lee, S. Huang, C. Wang, C. Wang, and S. Lu, "Design and analysis of a 21-29 GHz ultra-wideband receiver front-end in 0.18 μm CMOS technology," *IEEE Trans. Microw. Theory Tech.*, vol. 60, no. 8, pp. 2590–2604, Aug. 2012.

[7] A. Abbosh, "Ultra wideband inphase power divider for multi-layer technology," *IET Microw., Antennas, Propag.*, vol. 3, no. 1, pp. 148–153, 2009.

[8] J. Kao, Z. Tsai, K. Lin, and H. Wang, "A modified Wilkinson power divider with isolation bandwidth improvement," *IEEE Trans. Microw. Theory Tech.*, vol. 60, no. 9, pp. 2768–2780, Sep. 2012.

[9] M. Antoniades and G. Eleftheriades, "A broadband Wilkinson balun using microstrip metamaterial lines," *IEEE Microw. Wireless Propag. Lett.*, vol. 4, no. 1, pp. 209–212, Aug. 2005.

[10] J. Kim, M. Park, and M. Kim, "Out-of-phase Wilkinson power divider," *Electr. Lett.*, vol. 45, no. 1, pp. 59–60, 2009.

[11] S. Gruszczynski and K. Wincza, "Broadband rat-race couplers with coupled-line section and impedance transformers," *IEEE Microw. Propag. Lett.*, vol. 22, no. 1, pp. 22–24, Jan. 2012.

[12] H. Ahn and B. Kim, "Small wideband coupled-line ring hybrids with no restriction on coupling power," *IEEE Trans. Microw. Theory Tech.*, vol. 57, no. 7, pp. 1806–1817, Jul. 2009.

[13] T. Kim and B. Lee, "Metamaterial-based wideband rat-race hybrid coupler using slow wave lines," *IET Microw., Antennas, Propag.*, vol. 4, no. 6, pp. 717–721, 2010.

[14] M. Caillet, M. Clenet, A. Sharaiha, and Y. Antar, "A compact wide-band rat-race hybrid using microstrip lines," *IEEE Microw. Wireless Propag. Lett.*, vol. 19, no. 4, pp. 191–193, Apr. 2009.

[15] M. Mandal and S. Sanyal, "Reduced-length rat-race couplers," *IEEE Trans. Microw. Theory Tech.*, vol. 55, no. 12, pp. 2593–2598, Dec. 2007.

[16] A. Abbosh and M. Bialkowski, "Design of ultra wideband 3DB quadrature microstrip/slot coupler," *Microw. Opt. Tech. Lett.*, vol. 49, no. 9, pp. 2101–2103, 2007.

[17] M. Bialkowski and A. Abbosh, "Design of a compact UWB out of-phase power divider," *IEEE Microw. Wireless Propag. Lett.*, vol. 17, no. 4, pp. 289–291, Dec. 2007.

[18] G. Dai, X. Wei, E. Li, and M. Xia, "Novel dual-band out-of-phase power divider with high power-handling capability," *IEEE Trans. Microw. Theory Tech.*, vol. 60, no. 8, pp. 2403–2409, Aug. 2012.

[19] A. Abbosh and M. Bialkowski, "An UWB planar out-of-phase power divider employing parallel stripline-microstrip transitions," *Microw. Opt. Tech. Lett.*, vol. 49, no. 4, pp. 912–914, 2007.

[20] K. Eccleston, "Folded substrate-integrated waveguide out-of-phase power divider," in *Proc. Asia-Pacific Microw. Conf.*, Dec. 2010, pp. 1260–1263.

[21] H. Oraizi and A. Sharifi, "Optimum design of a wideband two-way Gysel power divider with source to load impedance matching," *IEEE Trans. Microw. Theory Tech.*, vol. 57, no. 9, pp. 2238–2248, Sep. 2009.

[22] Z. Sun, L. Zhang, Y. Liu, and X. Tong, "Modified Gysel power divider for dual-band applications," *IEEE Microw. Wireless Propag. Lett.*, vol. 21, no. 1, pp. 16–18, Jan. 2011.

[23] F. Lin, Q. Chu, Z. Gong, and Z. Lin, "Compact broadband Gysel power divider with arbitrary power-dividing ratio using microstrip/slotline phase inverter," *IEEE Trans. Microwave Theory Tech.*, vol. 60, no. 5, pp. 1226–1234, May 2012.

Amin M. Abbosh (SM'08) received the B.Sc. degree in electrical engineering, M.Sc. degree in communication systems, and Ph.D. degree in microwave engineering from Mosul University, Mosul, Iraq, in 1984, 1991, and 1996, respectively, the Higher Education in Grad Cert in 2008, and the D.Eng. degree from the University of Queensland, St Lucia, Australia, in 2013.

He currently holds the prestigious ARC Future Fellowship with the School of Information Technology and Electrical Engineering, University of Queensland, Queensland, Australia. He has authored more than 200 papers on wideband passive microwave devices, planar antennas, and microwave-based imaging systems.